REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Examiner's Final Action and respectfully requests reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicant originally submitted Claims 1-20 in the application. The Applicant previously amended Claims 1, 8 and 15. In the current response, the Applicant amends Claims 1, 8 and 15. Accordingly, Claims 1-20 are currently pending in the application.

I. Rejection of Claims 1-20 under 35 U.S.C. § 102

The Examiner has rejected Claims 1-20 under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent 5,651,125 to Witt, *et al.* The Applicant respectfully traverses the Examiner's rejection, because Witt does not teach or suggest each and every element of the presently claimed invention. Specifically, with respect to claims 1, 8 and 15, Witt fails to teach or suggest queuing logic in which instructions and instruction type information are stored in an order based on a priority of the instructions derived from rules that reduce resource allocation conflicts in a processor.

Witt is directed in general to microprocessors and, more particularly, to high performance superscalar microprocessors. (Col. 2, lines 51-53.) Witt teaches certain well-known concepts related to microprocessor architecture, including decoding of instructions to generate an opcode, and queuing of the opcode and instruction tags in a reservation station at the input to a functional unit. (See, *e.g.*, column 5, lines 19-40; column 13, lines 22-56.)

However, Witt does not teach that that instructions and instruction type information are stored in an order based on a priority of said instructions derived from a priority of functional units in

a processor, as recited in Claims 1, 8 and 15. The Examiner in her November 17, 2005, Action notes that instructions are stored in the reservation stations based on age, where age may be considered a priority. Accepting the Examiner's position *arguendo*, while reserving judgment on the issue, such a queuing method does not store instructions in an order based on a priority of said instructions derived from a priority of functional units in a processor. Instead, the instructions are stored in an order that they are issued by the processor. Moreover, those of ordinary skill in the art recognize that such storage in a reservation station is not equivalent to the element at issue because a reservation station is designed to merely wait until a functional unit becomes available to execute an instruction, but does not do so based on a priority of functional units in the processor. Therefore, Witt does not anticipate this element, and Claims 1, 8 and 15, and those claims depending therefrom, are novel over Witt.

Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection under 35 U.S.C §102(b) and allow Claims 1-20.

II. Conclusion

In view of the foregoing amendments and remarks, the Applicant now sees all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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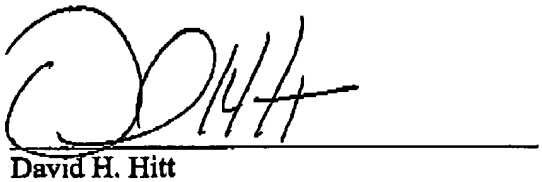

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